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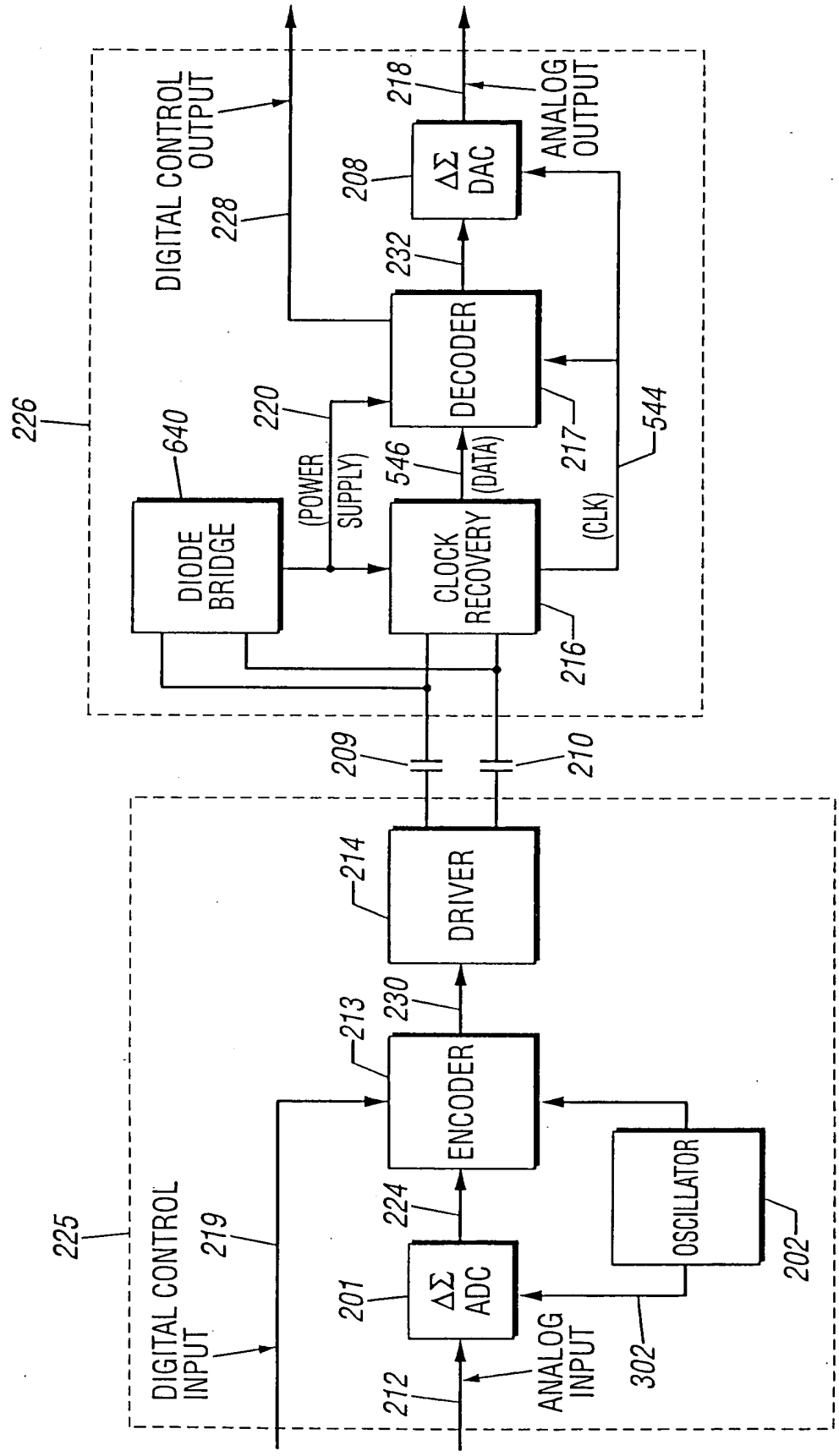


FIG. 2

FIG. 3A

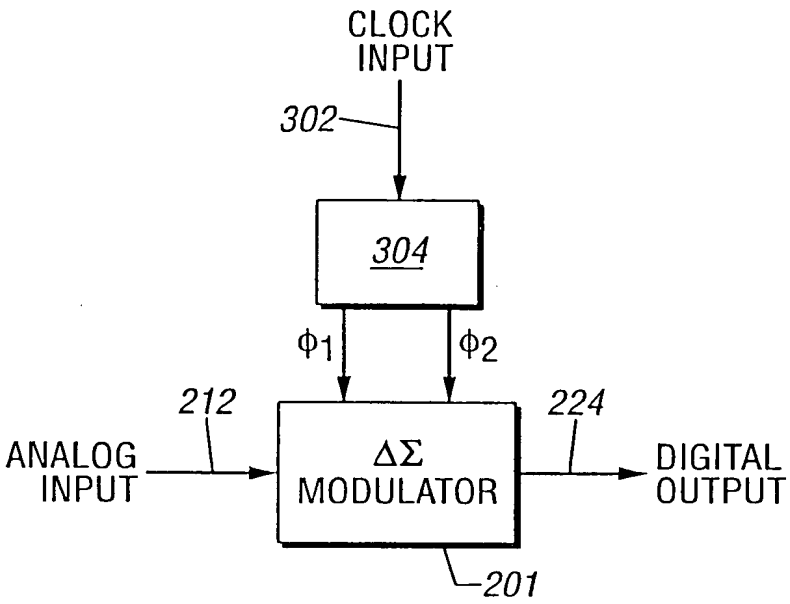

CLOCK
INPUT
302
304
Φ1
Φ2
212
224
ANALOG
INPUT
ΔΣ
MODULATOR
DIGITAL
OUTPUT
201

FIG. 3B

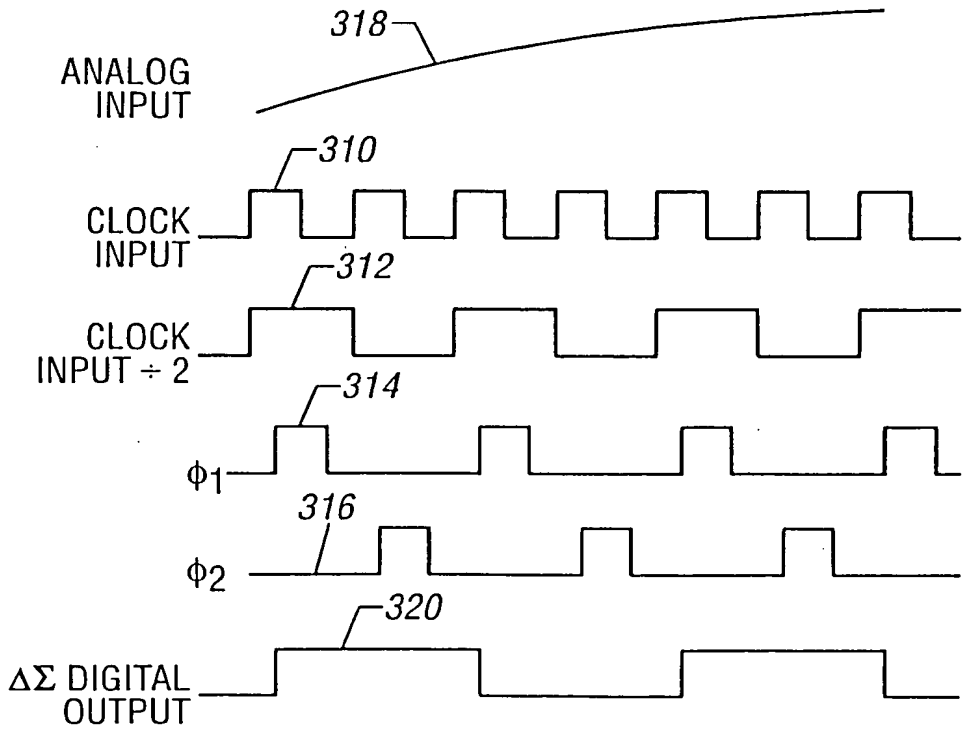

318
ANALOG
INPUT
310
CLOCK
INPUT
312
CLOCK
INPUT ÷ 2
314
Φ1
316
Φ2
320
ΔΣ DIGITAL
OUTPUT

FIG. 4A

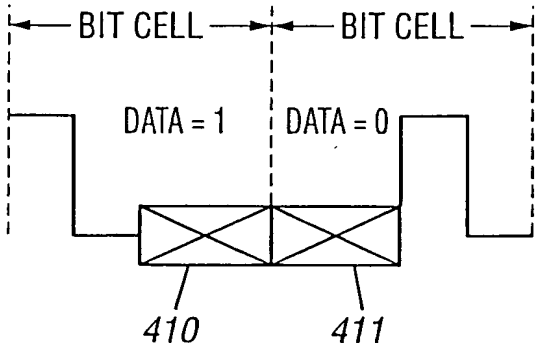


FIG. 4B

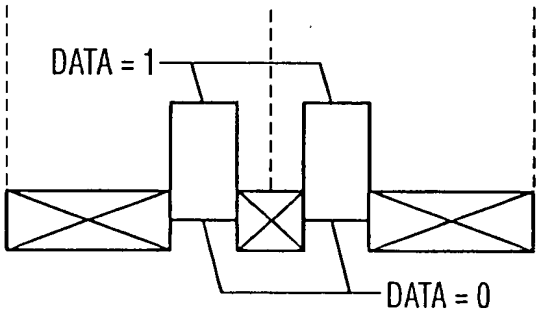


FIG. 5

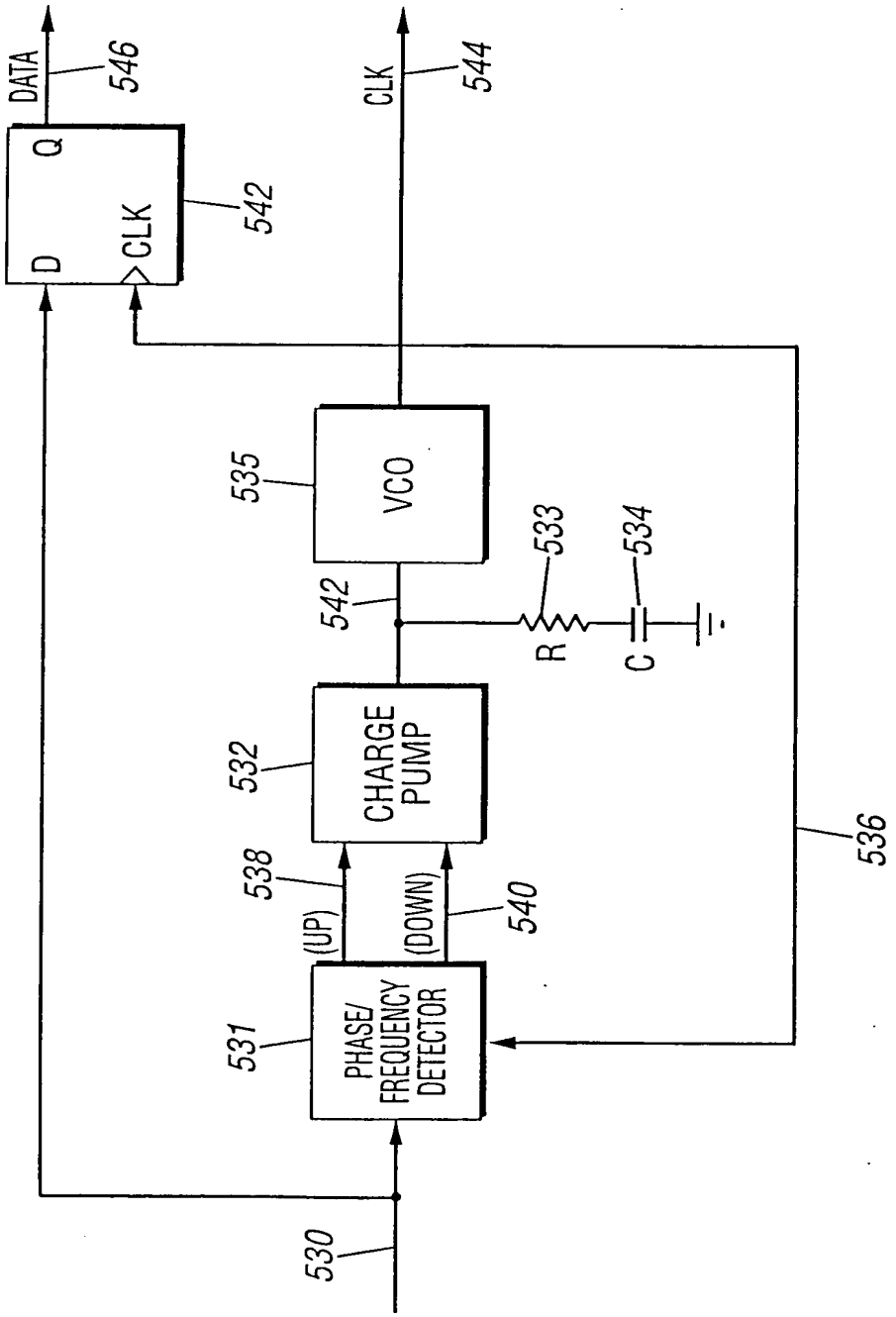

DATA
546
CLK
544
Q
D
CLK
542
535
VCO
533
534
542
R
C
532
CHARGE PUMP
538
(UP)
(DOWN)
540
536
531
PHASE/ FREQUENCY DETECTOR
530

FIG. 6A

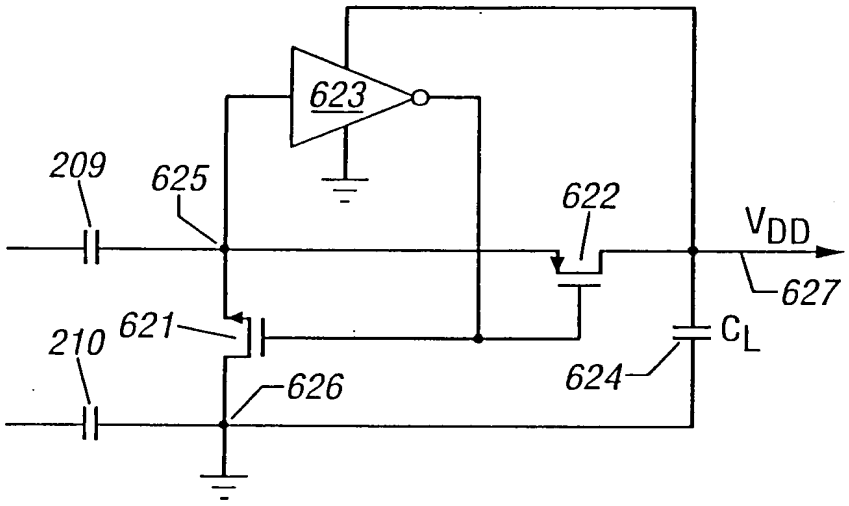

623
209
625
622
V_{DD}
627
210
621
C_L
624
626

FIG. 6B

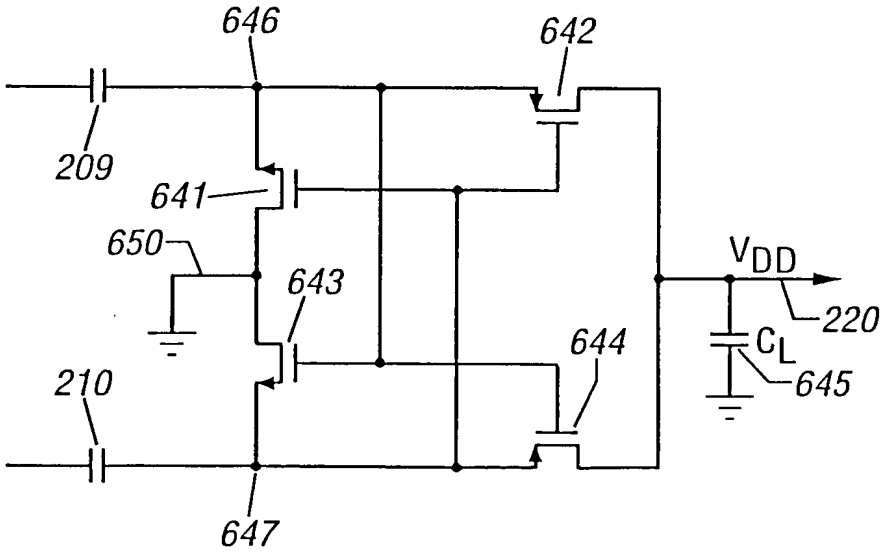
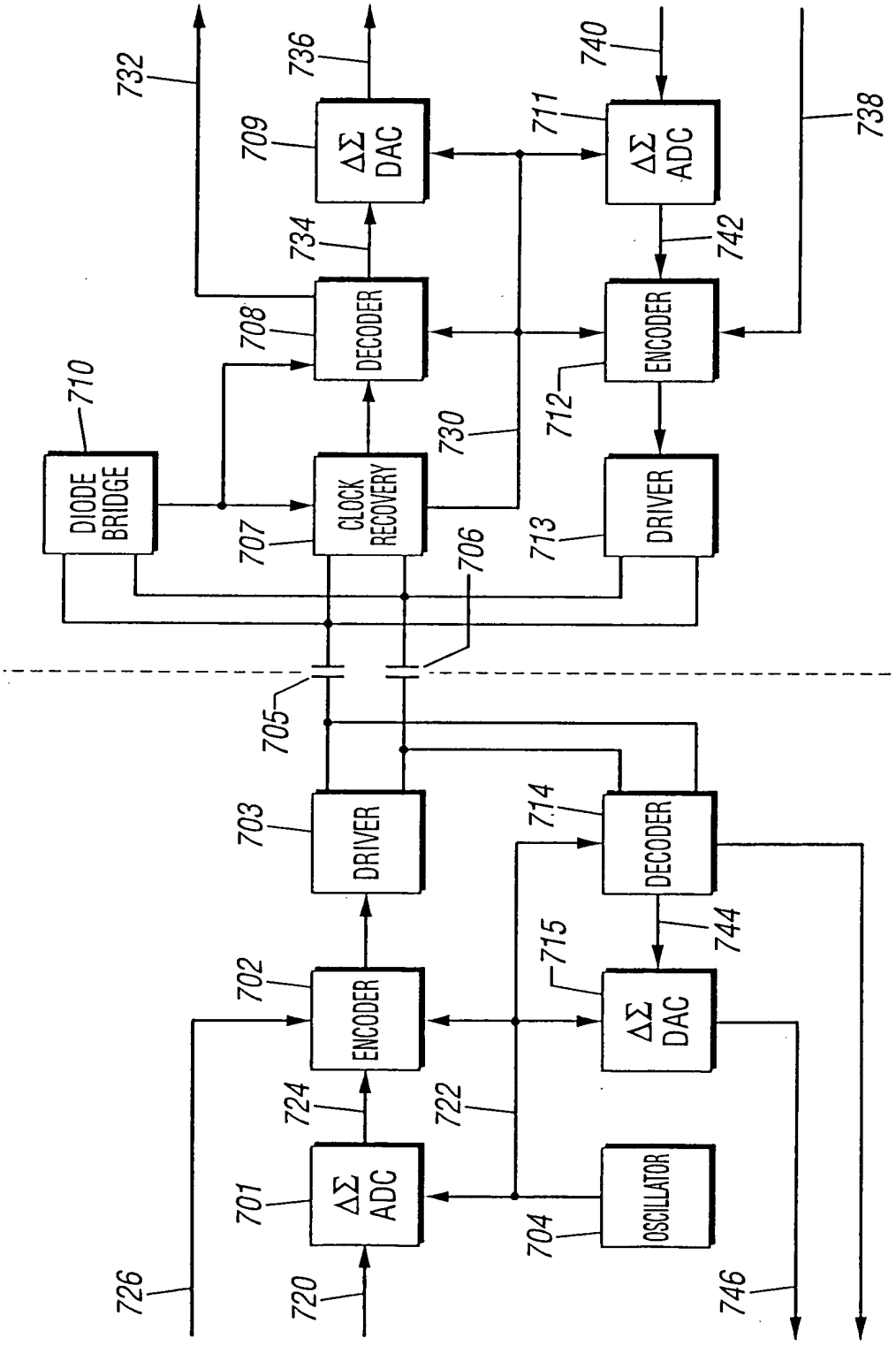

646
642
209
641
650
643
V_{DD}
220
644
C_L
645
210
647

FIG. 7


732
736
740
709
ΔΣ DAC
711
ΔΣ ADC
738
734
742
708
DECODER
ENCODER
710
730
712
DIODE BRIDGE
CLOCK RECOVERY
DRIVER
707
706
713
705
703
DRIVER
714
DECODER
744
715
702
ENCODER
ΔΣ DAC
724
722
701
ΔΣ ADC
OSCILLATOR
704
726
720
746

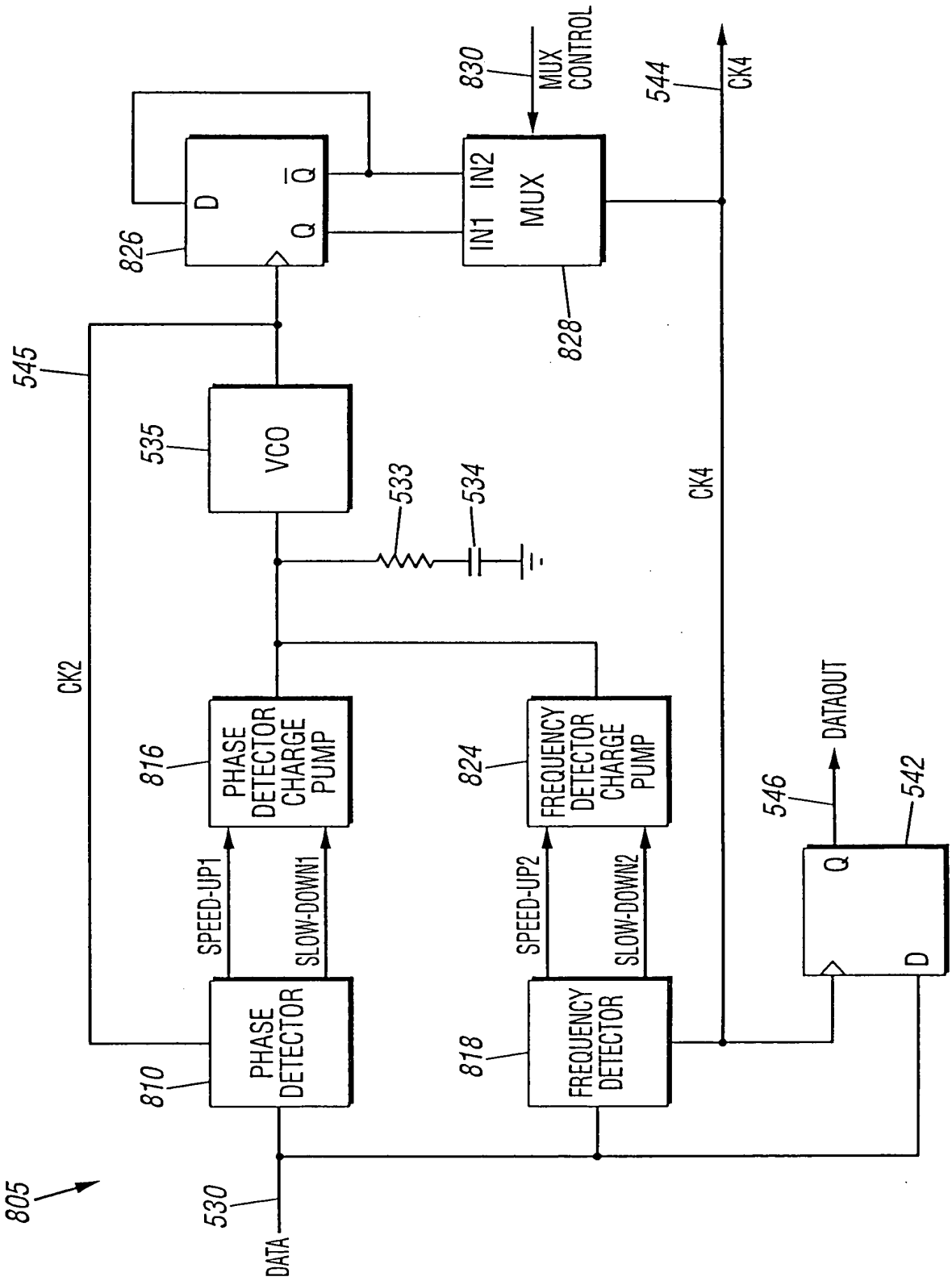
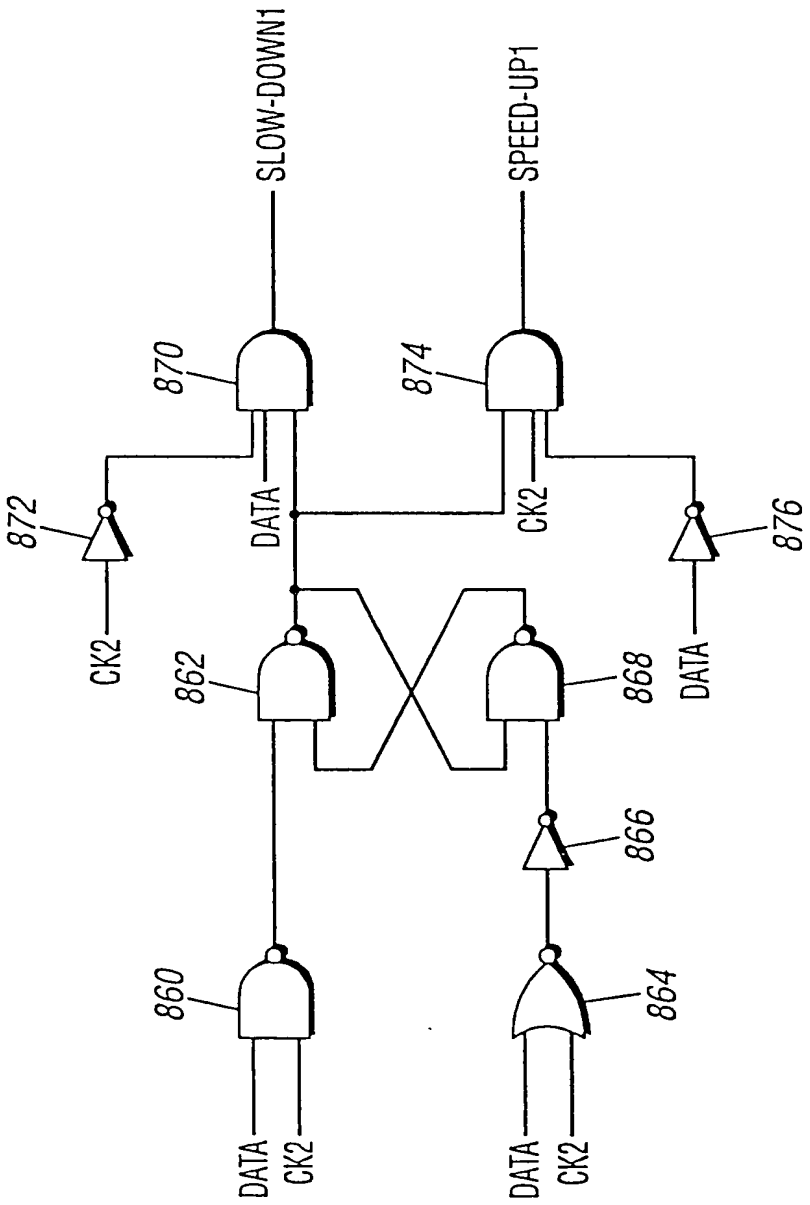

805
530
DATA
810
PHASE DETECTOR
818
FREQUENCY DETECTOR
816
PHASE DETECTOR CHARGE PUMP
824
FREQUENCY DETECTOR CHARGE PUMP
SPEED-UP1
SLOW-DOWN1
SPEED-UP2
SLOW-DOWN2
CK2
545
535
VCO
533
534
826
D
Q
$\bar{Q}$
828
IN1
IN2
MUX
830
MUX CONTROL
544
CK4
CK4
546
542
DATAOUT
Q
D

FIG. 8

FIG. 9


SLOW-DOWN1
SPEED-UP1
870
874
872
DATA
CK2
876
CK2
862
868
DATA
866
860
864
DATA
CK2
DATA
CK2

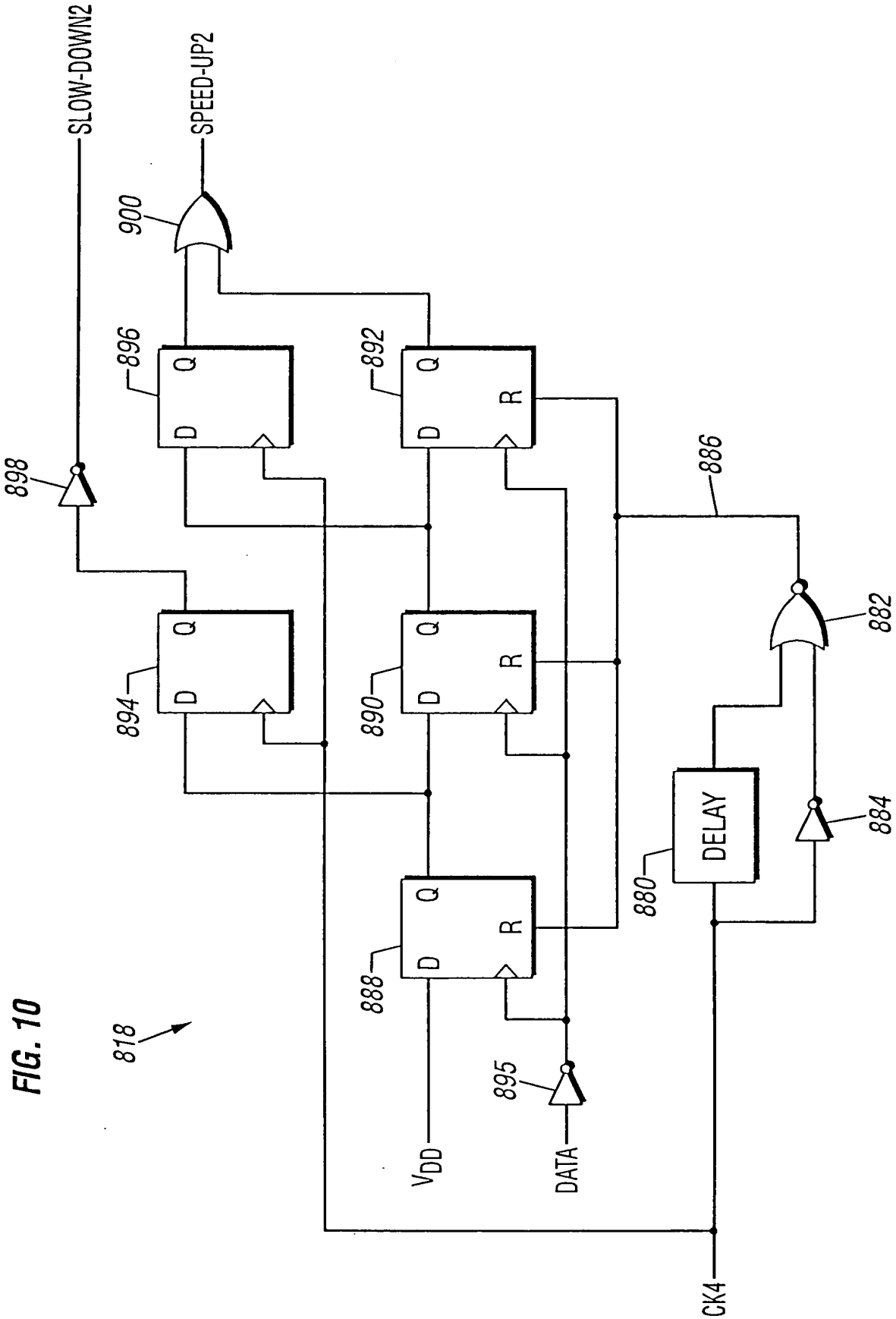

SLOW-DOWN2
SPEED-UP2
900
896
892
898
886
894
890
882
884
DELAY
880
888
818
895
V_{DD}
DATA
CK4

FIG. 10

FIG. 11

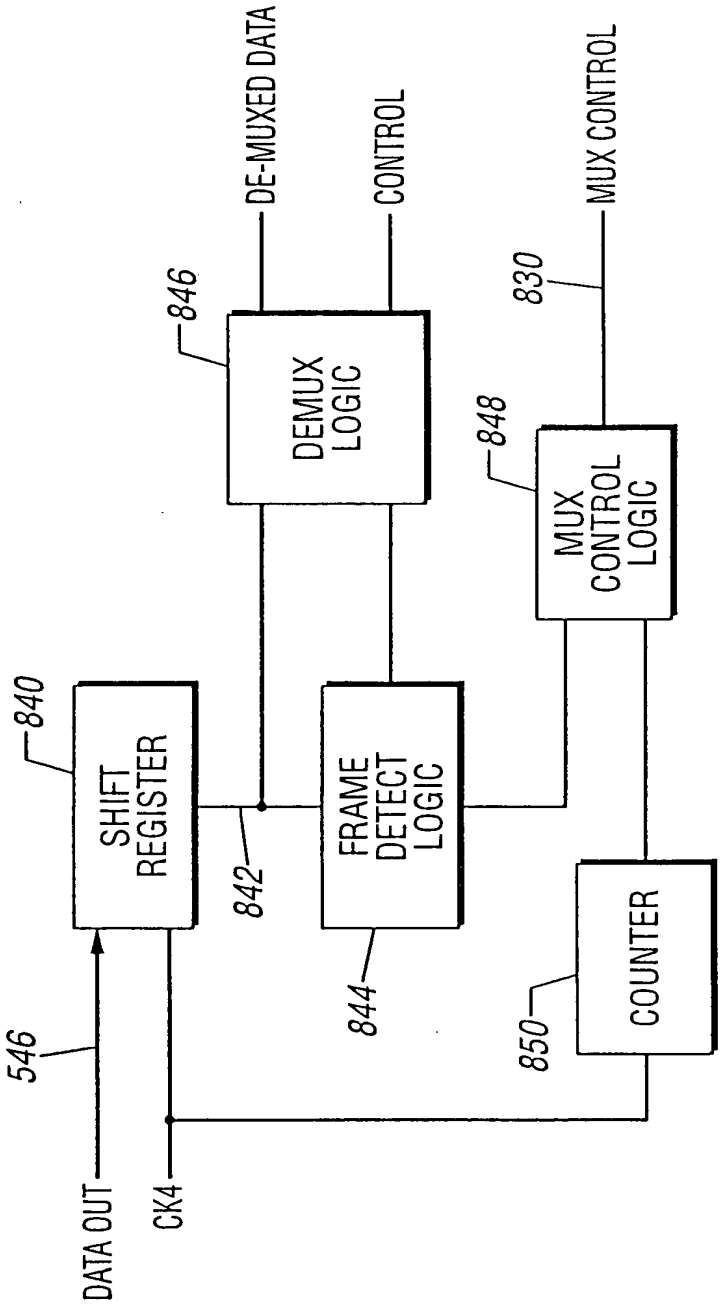

DE-MUXED DATA
CONTROL
MUX CONTROL
846
830
848
DEMUX LOGIC
MUX CONTROL LOGIC
840
SHIFT REGISTER
842
FRAME DETECT LOGIC
844
COUNTER
850
546
DATA OUT
CK4

FIG. 12

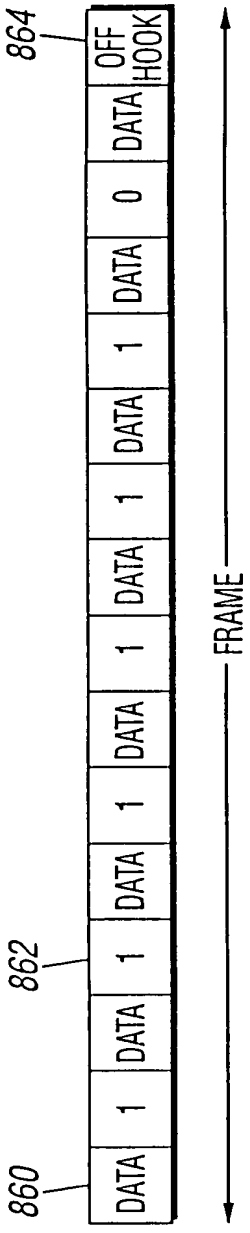

864
OFF HOOK
DATA
0
DATA
1
DATA
1
DATA
1
DATA
1
DATA
1
DATA
1
DATA
862
860
FRAME

FIG. 13B

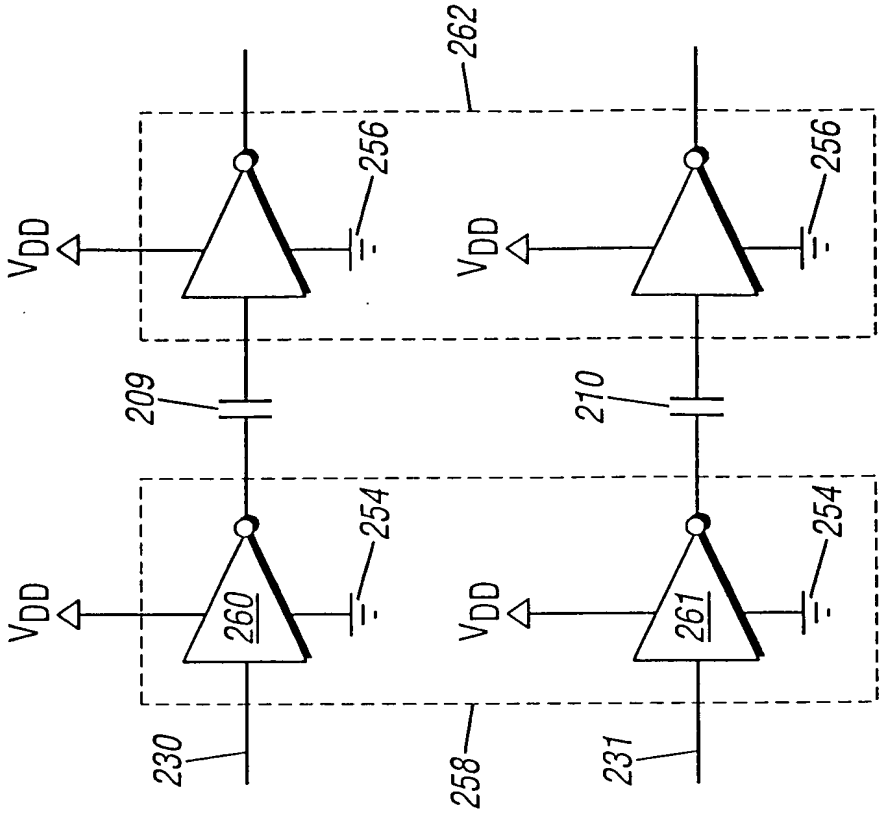


FIG. 13A

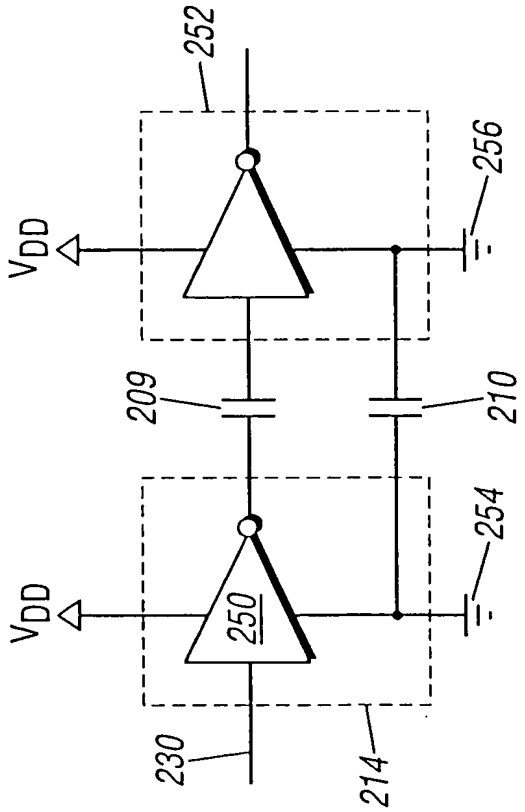


FIG. 14

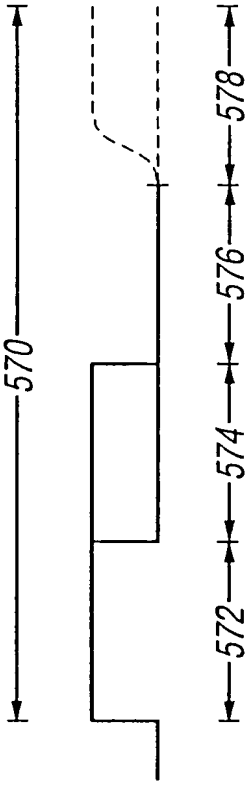
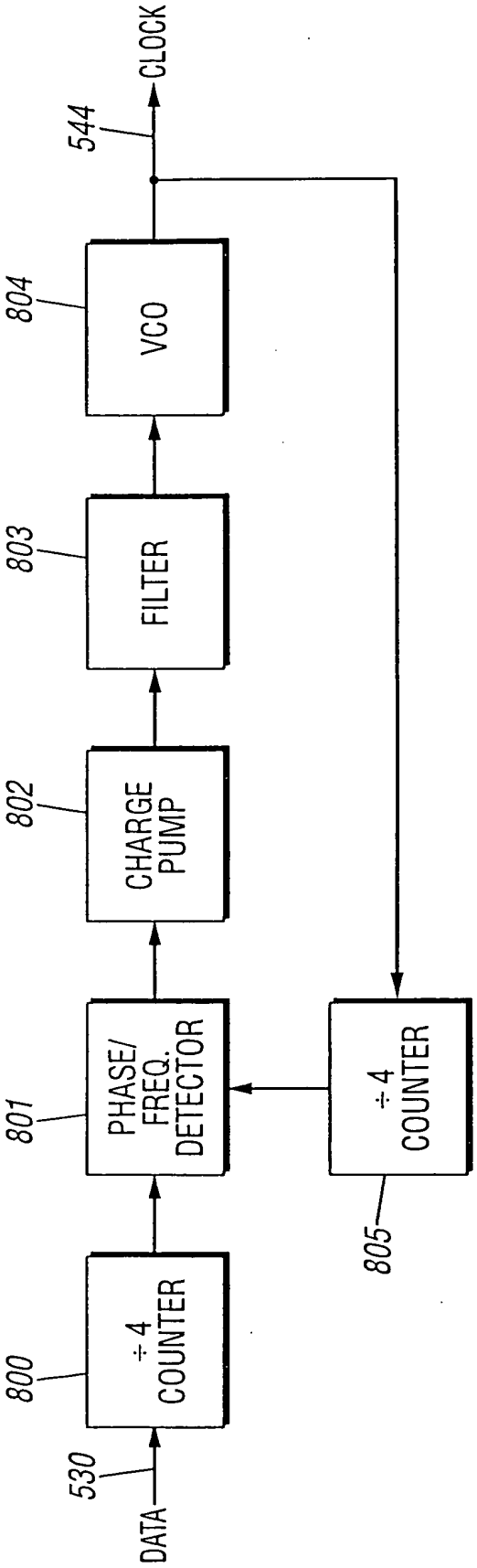

570
572
574
576
578

FIG. 15


DATA
530
800
÷4 COUNTER
801
PHASE/ FREQ. DETECTOR
802
CHARGE PUMP
803
FILTER
804
VCO
544
CLOCK
805
÷4 COUNTER

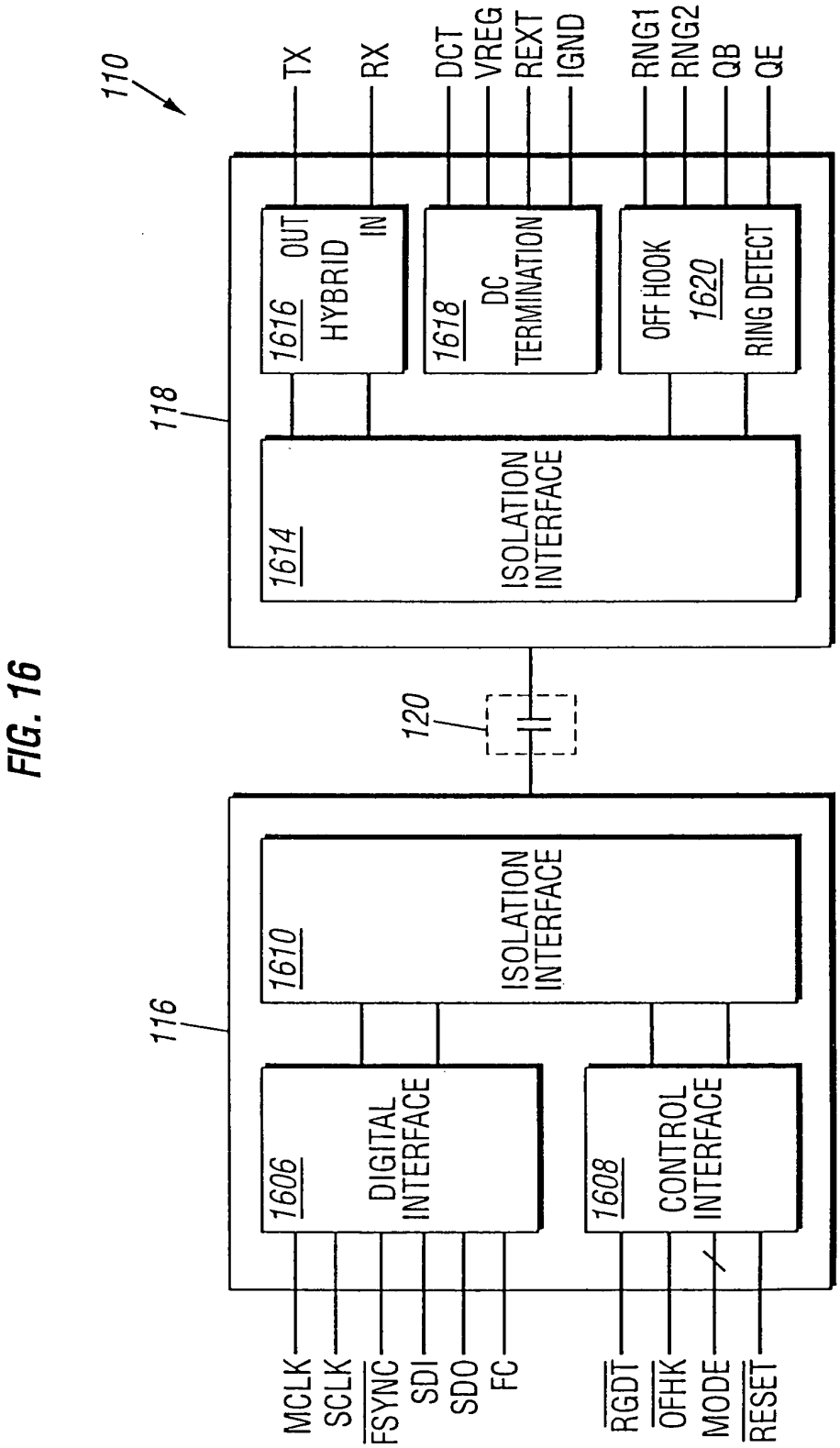

110
TX
RX
DCT
VREG
REXT
IGND
RNG1
RNG2
QB
QE
118
1616 OUT
HYBRID
IN
1618
DC
TERMINATION
OFF HOOK
1620
RING DETECT
1614
ISOLATION
INTERFACE
120
116
1610
ISOLATION
INTERFACE
1606
DIGITAL
INTERFACE
1608
CONTROL
INTERFACE
MCLK
SCLK
FSYNC
SDI
SDO
FC
RGDT
OFHK
MODE
RESET

FIG. 16

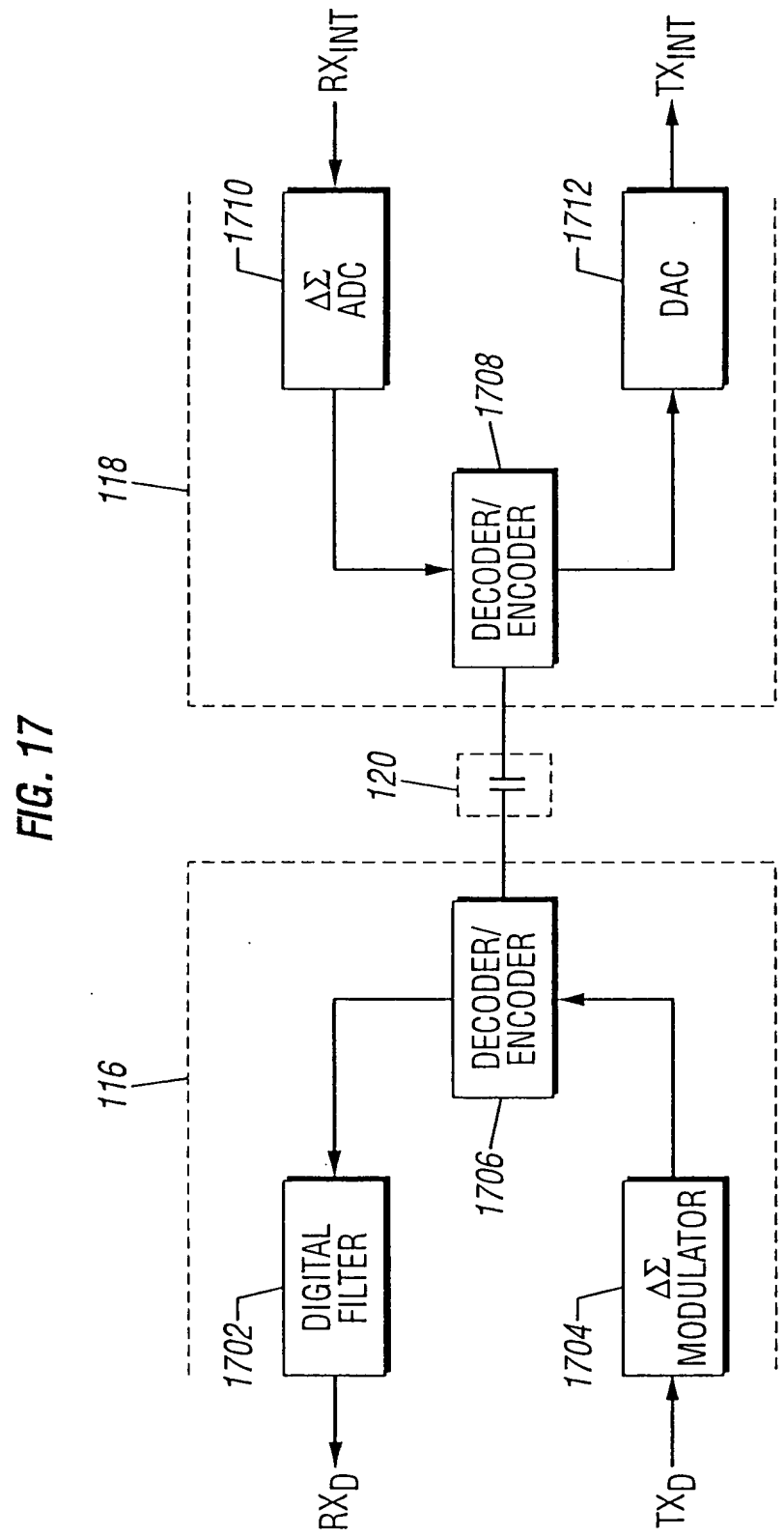
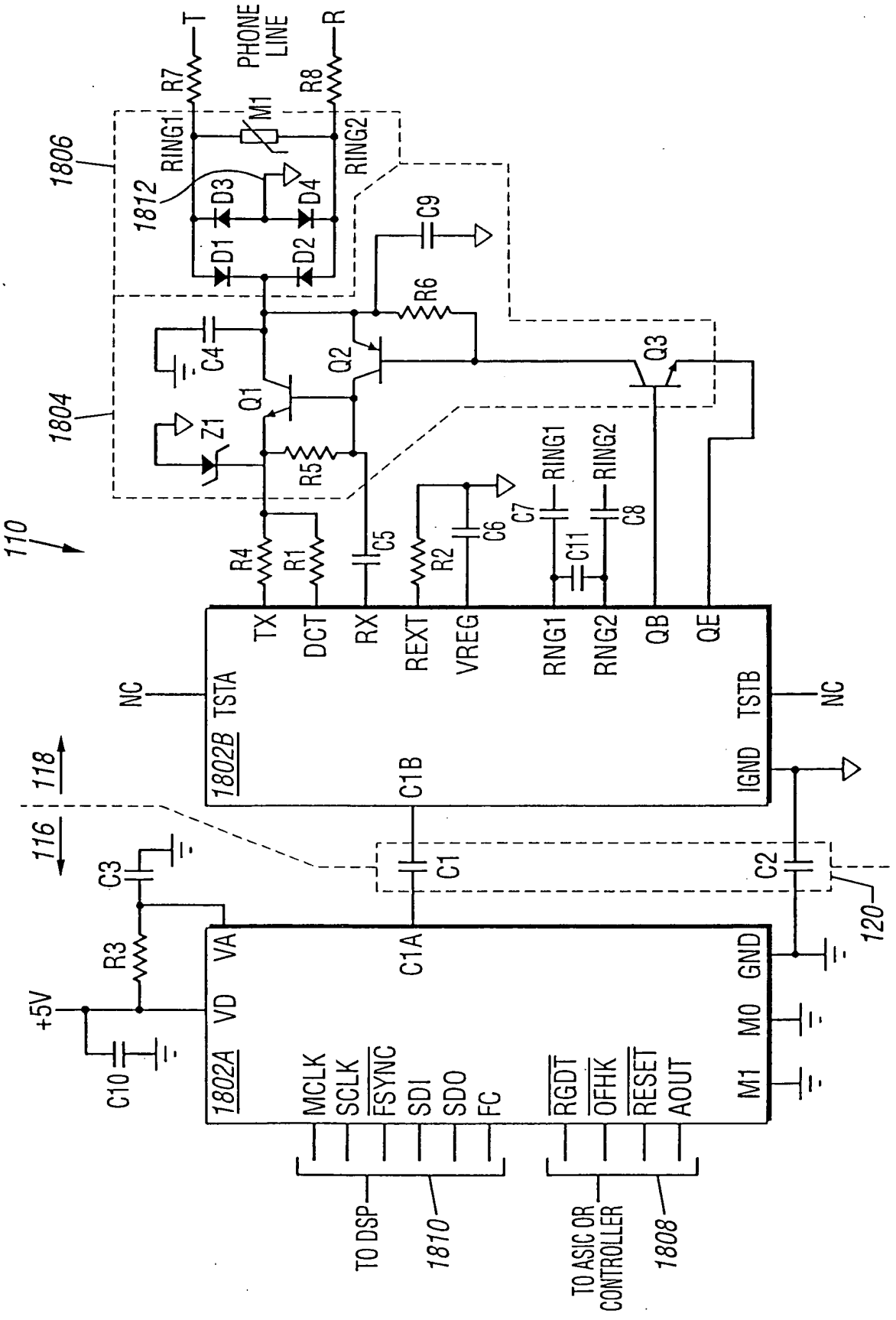

RX_INT
TX_INT
1710
ΔΣ ADC
1712
DAC
118
1708
DECODER/ ENCODER
120
116
DECODER/ ENCODER
1706
1702
DIGITAL FILTER
1704
ΔΣ MODULATOR
RX_D
TX_D

FIG. 17

FIG. 18


110
1806
1812
1804
PHONE LINE
T
R
R7
R8
M1
RING1
RING2
D1
D2
D3
D4
C9
R6
C4
Q1
Q2
Q3
Z1
R5
R4
R1
C5
R2
C6
C7
C11
C8
RING1
RING2
TX
DCT
RX
REXT
VREG
RNG1
RNG2
QB
QE
NC
TSTA
1802B
TSTB
NC
IGND
118
116
C1B
C1
C2
120
C3
R3
+5V
C10
VA
VD
1802A
C1A
GND
M0
M1
MCLK
SCLK
FSYNC
SDI
SDO
FC
RGDT
OFHK
RESET
AOUT
TO DSP
1810
TO ASIC OR CONTROLLER
1808

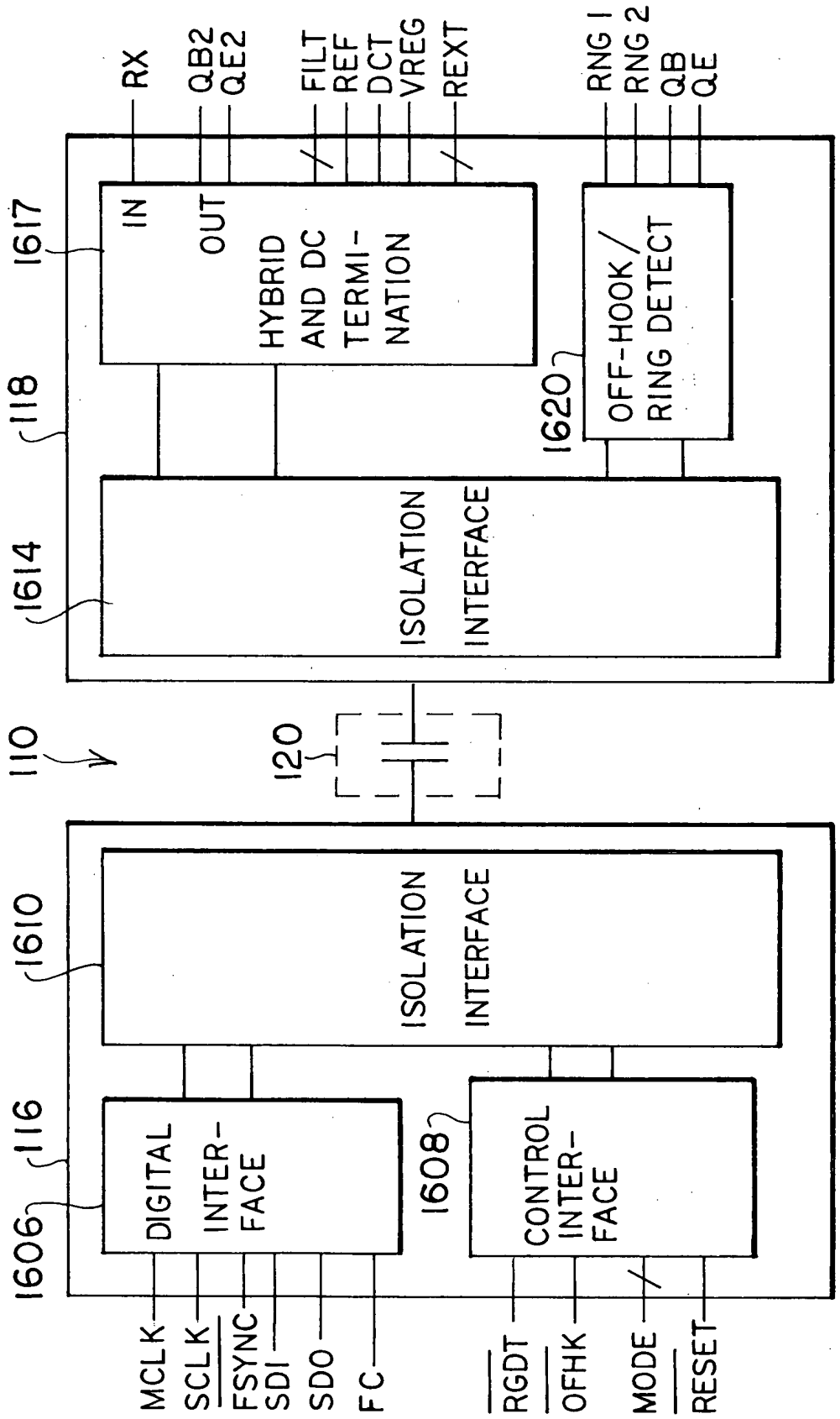

RX
QB2
QE2
FILT
REF
DCT
VREG
REXT
RNG 1
RNG 2
QB
QE
1617
IN
OUT
HYBRID AND DC TERMI-NATION
1620
OFF-HOOK / RING DETECT
118
1614
ISOLATION INTERFACE
110
120
1610
ISOLATION INTERFACE
116
1606
DIGITAL INTER-FACE
1608
CONTROL INTER-FACE
MCLK
SCLK
FSYNC
SDI
SDO
FC
RGDT
OFHK
MODE
RESET

FIG. 19

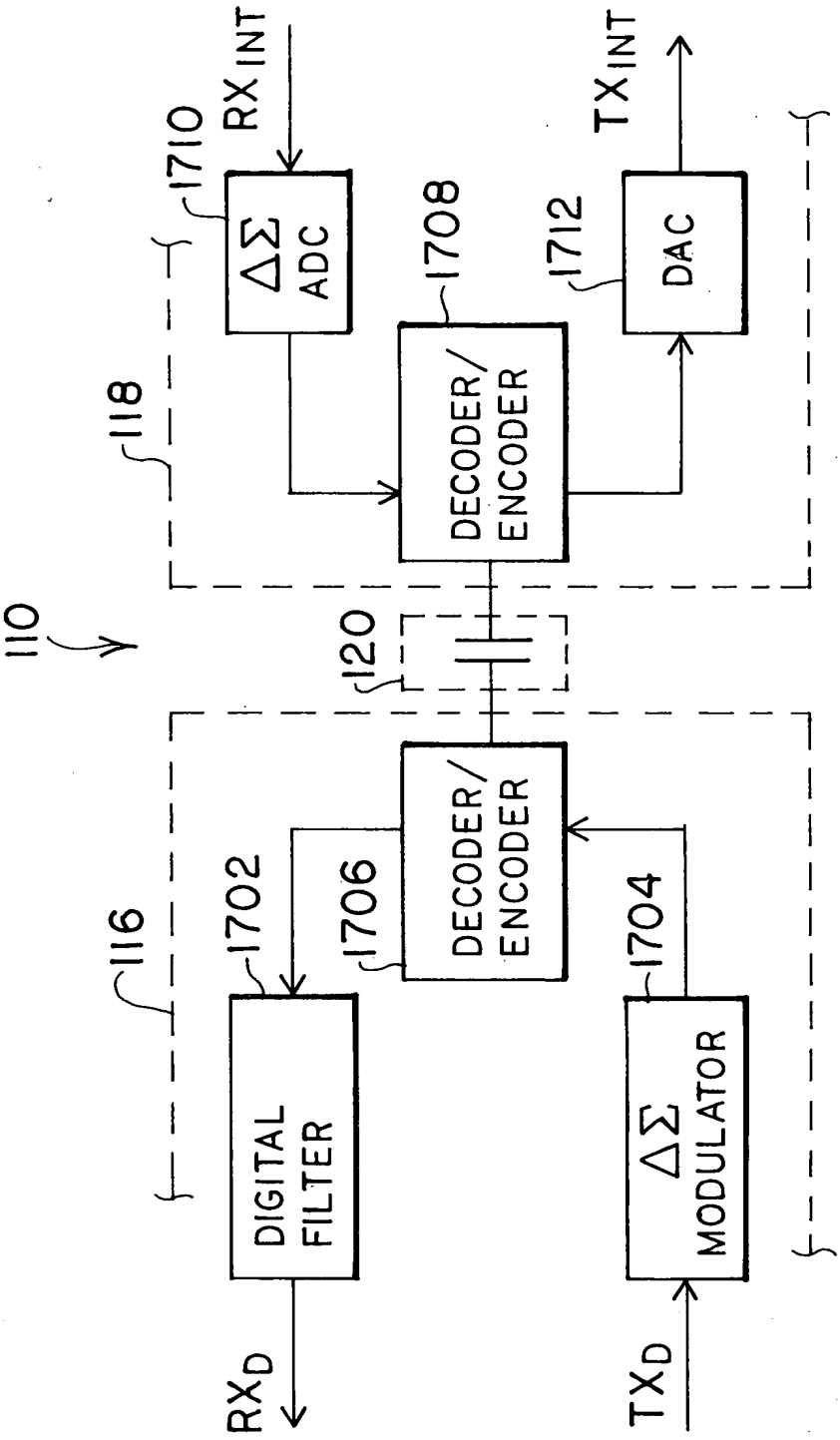

110
118
116
120
1710
RX INT
ΔΣ ADC
1708
DECODER/ ENCODER
1712
DAC
TX INT
1702
1706
DECODER/ ENCODER
1704
DIGITAL FILTER
ΔΣ MODULATOR
RXD
TXD

FIG. 20

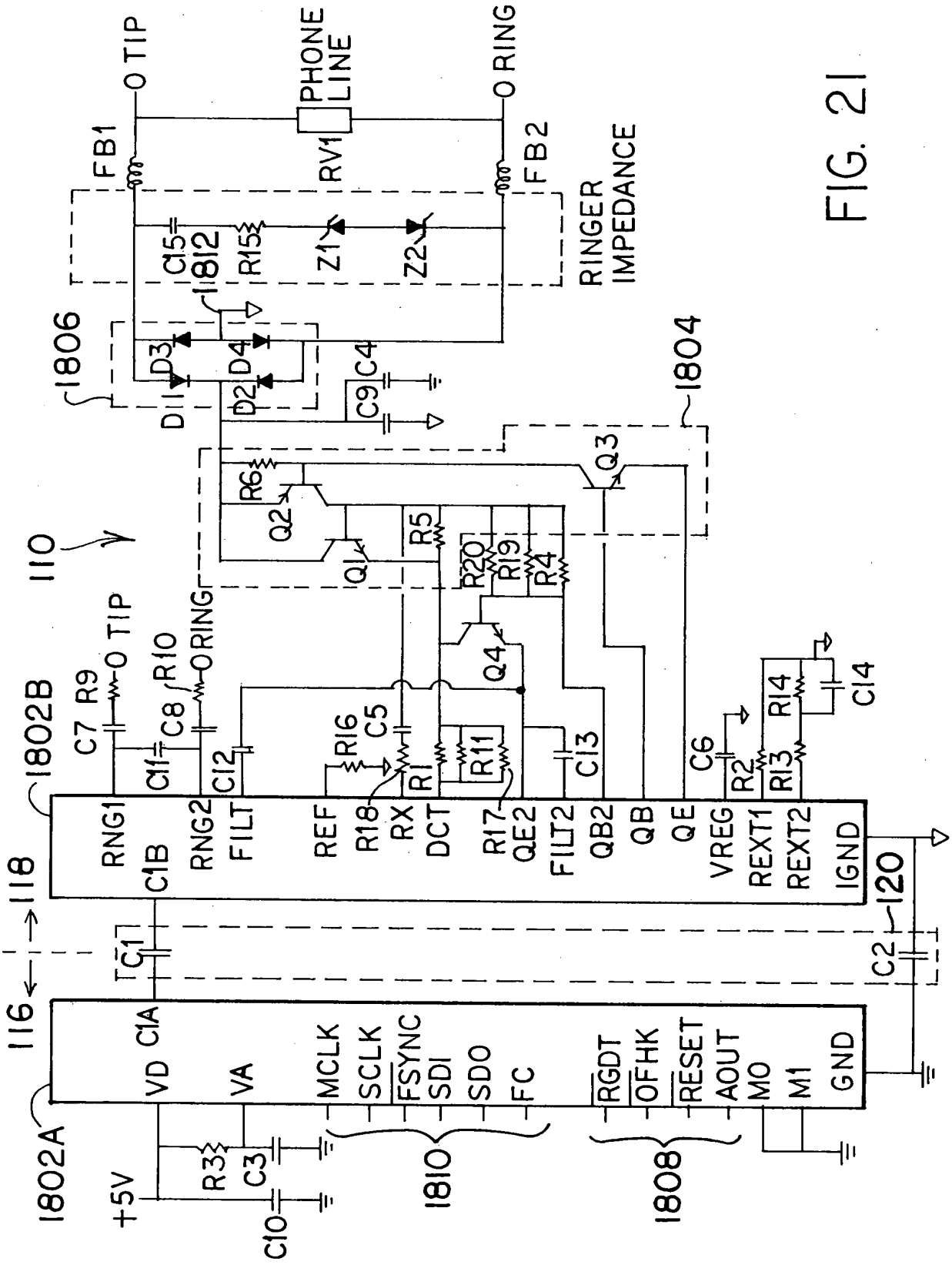

TIP
RING
PHONE LINE
FB1
FB2
RV1
RINGER IMPEDANCE
1812
1806
1804
1802B
1802A
110
118
116
120
1810
1808
+5V
C15
R15
Z1
Z2
D3
D4
D1
D2
C4
C9
Q1
Q2
Q3
Q4
R6
R5
R20
R19
R4
R10
R9
C7
C8
C11
C12
R16
C5
R1
R11
C13
C6
R2
R13
R14
C14
C1
C2
C10
R3
C3
RNG1
C1B
RNG2
FILT
REF
R18
RX
DCT
R17
QE2
FILT2
QB2
QB
QE
VREG
REXT1
REXT2
IGND
VD
C1A
VA
MCLK
SCLK
FSYNC
SDI
SDO
FC
RGDT
OFHK
RESET
AOUT
M0
M1
GND

FIG. 21

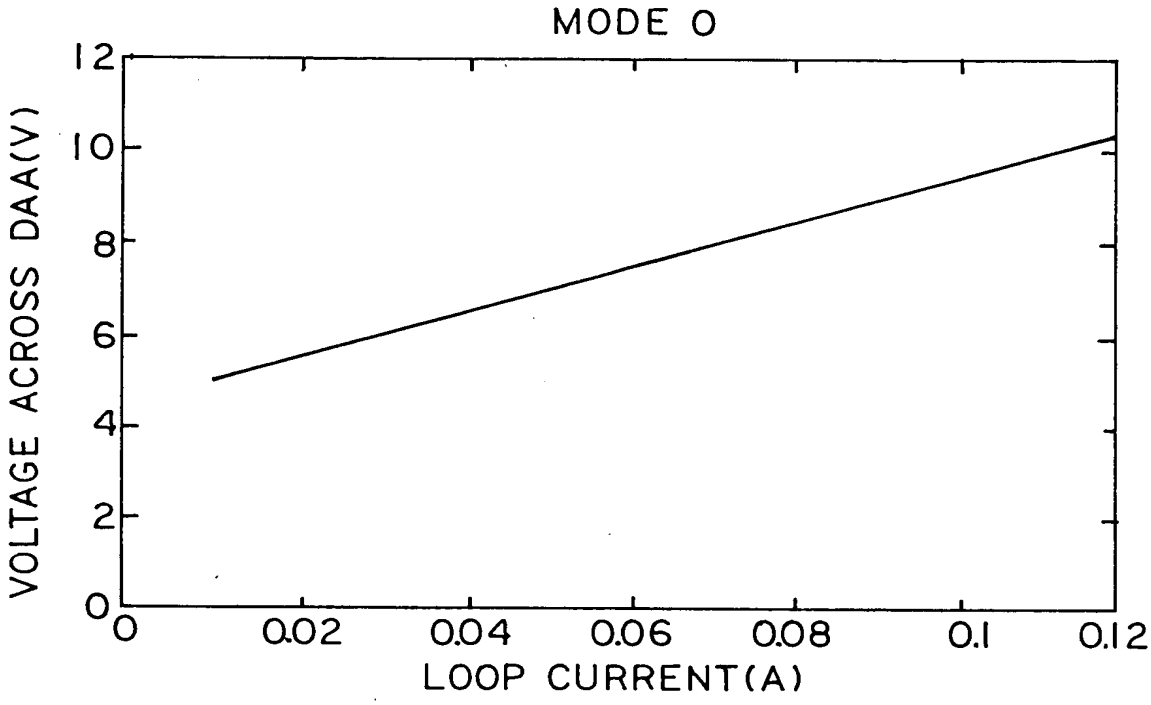


FIG. 22A

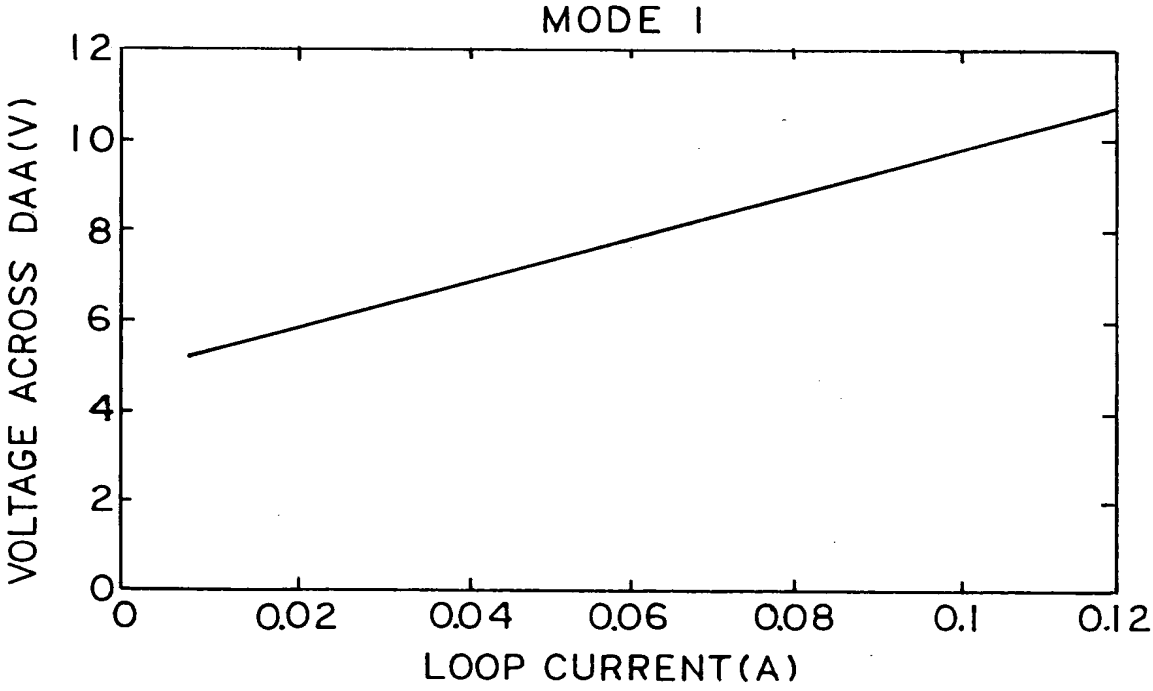


FIG. 22B

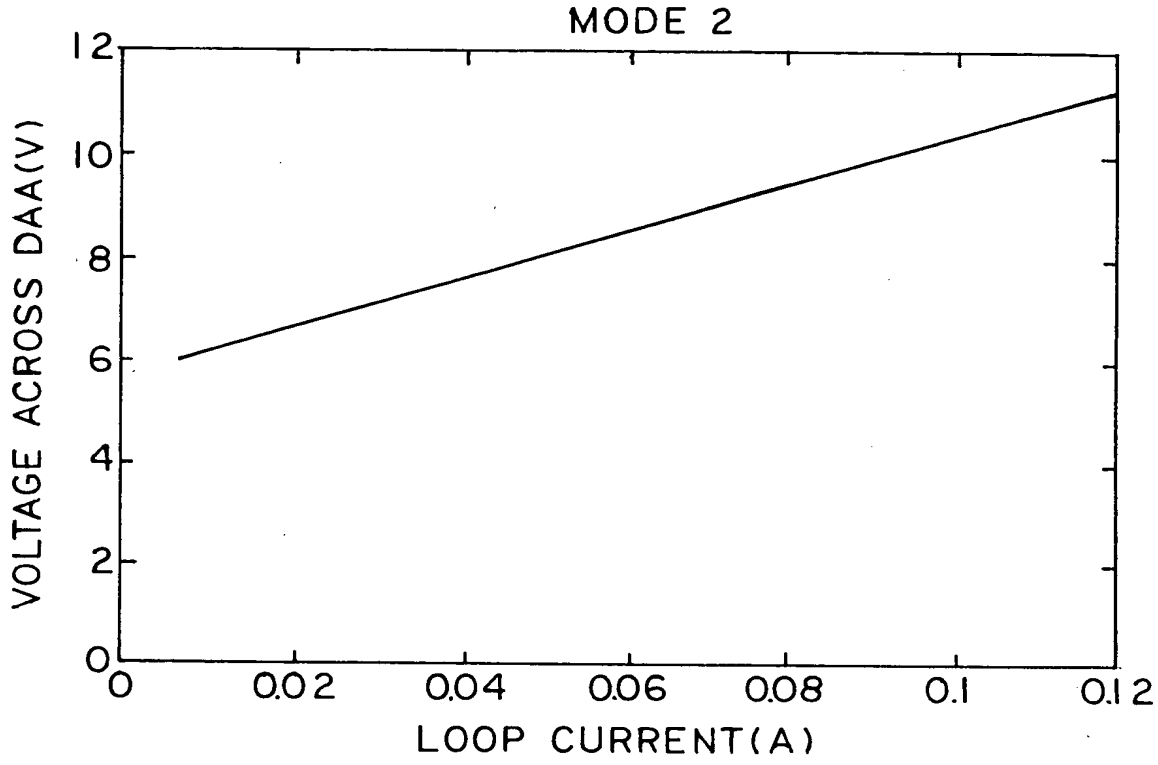


FIG. 22C

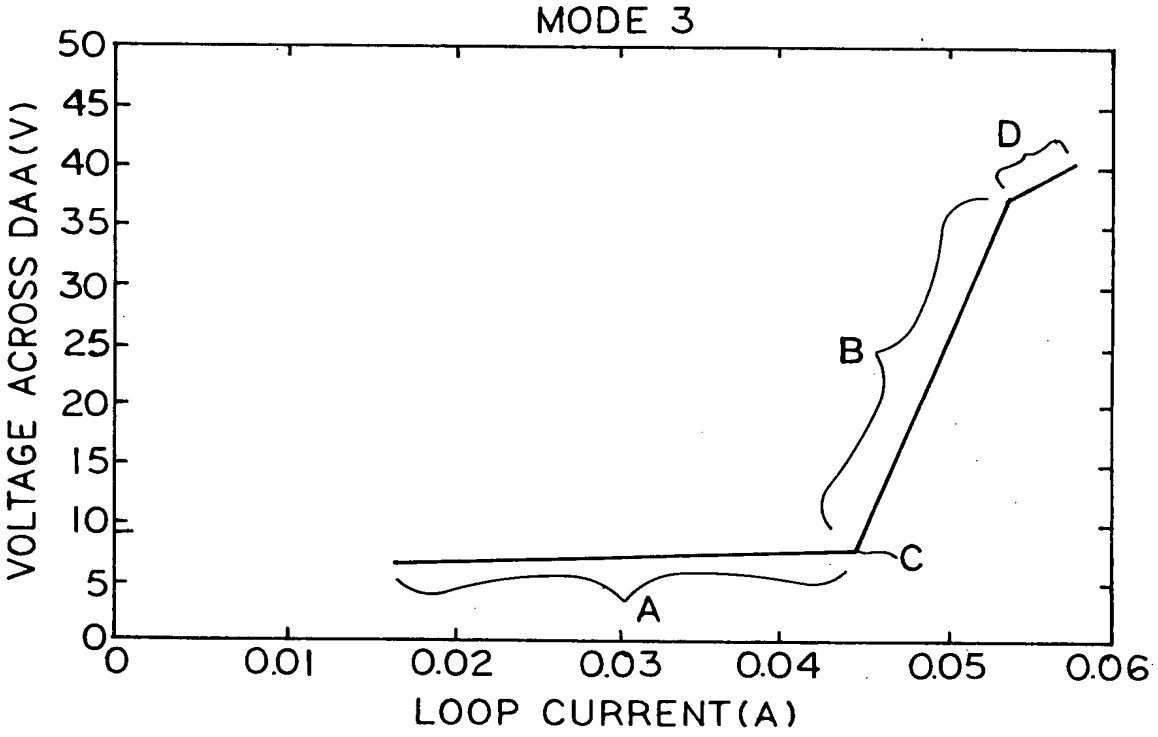


FIG. 22D

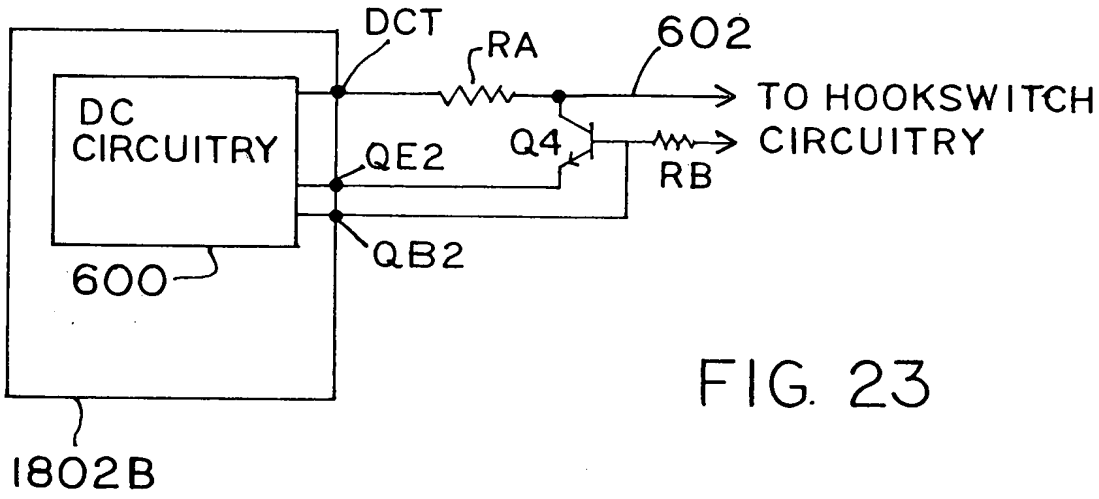

DCT
RA
602
DC
CIRCUITRY
TO HOOKSWITCH
CIRCUITRY
QE2
Q4
RB
QB2
600
1802B

FIG. 23

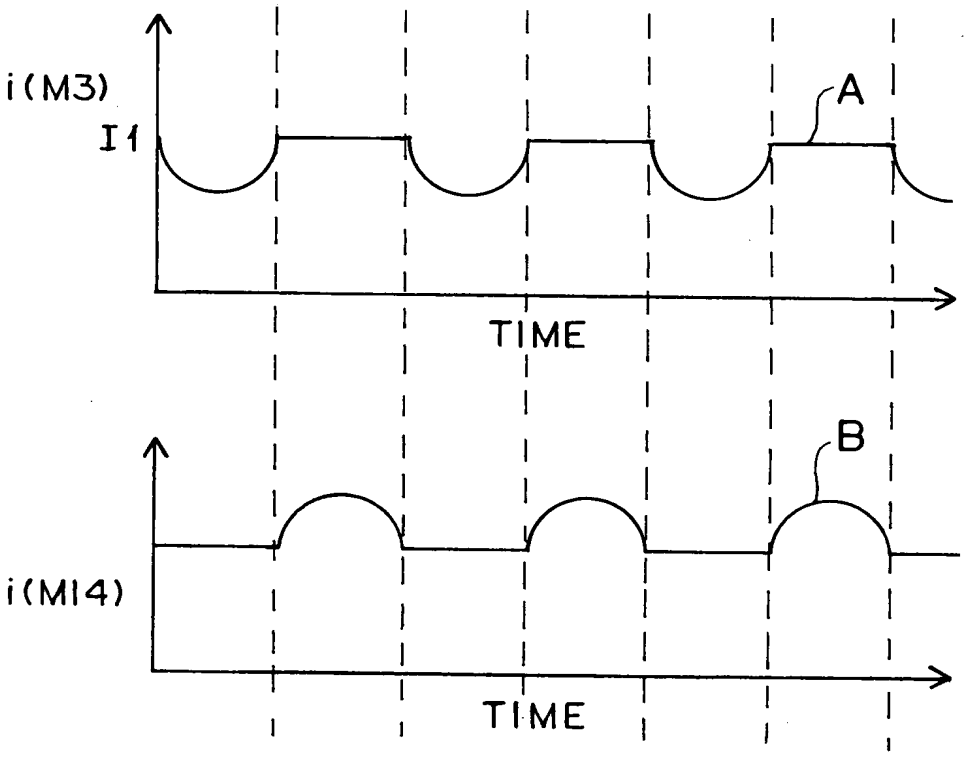

i(M3)
I1
A
TIME
B
i(M14)
TIME

FIG. 25

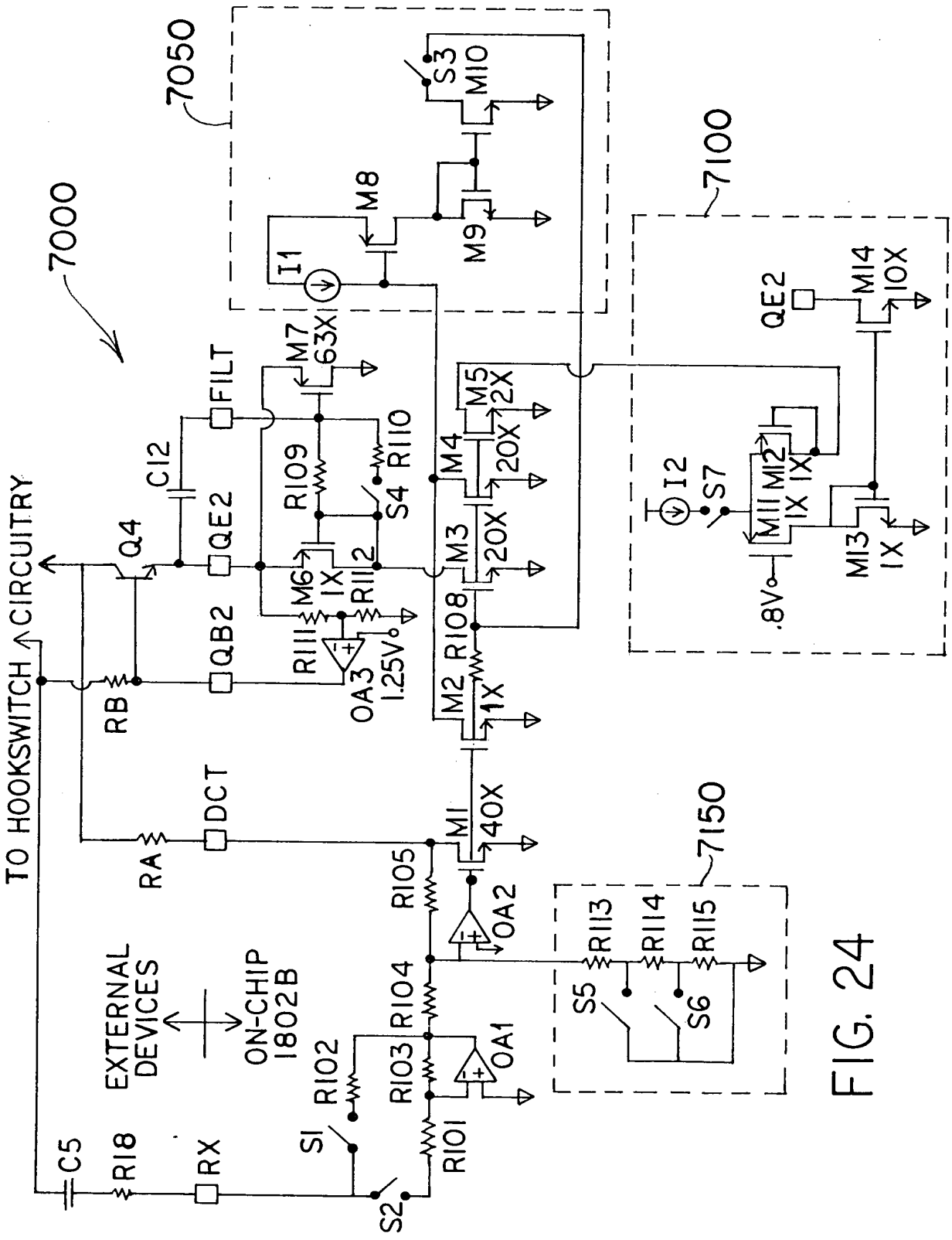

7000
7050
7100
7150
TO HOOKSWITCH CIRCUITRY
EXTERNAL DEVICES
ON-CHIP 1802B
FILT
QE2
QB2
DCT
RX
RA
RB
C12
C5
R18
Q4
M7 63X
M8
M9
M10
S3
I1
M5 2X
M4 20X
M3 20X
M2 1X
M1 40X
R109
R110
R111
R112
R108
M6 1X
S4
OA3 1.25V
R105
R104
R103
R102
R101
S1
S2
OA2
OA1
R113
R114
R115
S5
S6
I2
S7
M11
M12 1X
M13 1X
M14 10X
QE2
.8V

FIG. 24